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EXAMINER	
MAIS, MARK A	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/779,466	MORRIS, MATT	
	Examiner	Art Unit	
	MARK A. MAIS	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23 and 32-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23 and 32-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the function and location of a packet replicator in order to transmit replicated packets to multiple output ports/destinations (for multicast/broadcast transmissions). For example, are the packets replicated at the input storage? Are they replicated by the assignment data structure? Or the packet allocation data structure? Claims 2-7 are also rejected since they depend from claim 1 and contain the same deficiency.

3. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the function and location of a packet replicator in order to transmit

replicated packets to multiple output ports/destinations (for multicast/broadcast transmissions). For example, are the packets replicated at the input storage? Are they replicated by the assignment data structure? Or the packet allocation data structure? Claims 9-10 are also rejected since they depend from claim 8 and contain the same deficiency.

4. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: replicating the held packet in order to transmit replicated packets to multiple output ports/destinations (for multicast/broadcast transmissions). For example, are the packets replicated after holding each packet in a storage means? Are they replicated after the assignment data structure identifies the destination? Or are they replicated after packet allocation data structure identifies the address where the packet is held? Claims 12-14 are also rejected since they depend from claim 11 and contain the same deficiency.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Chapman et al. in view of Barnes et al. further in view of Wegner et al.

6. Claims 1-14 and 32-35 are rejected under 35 U.S.C. 102(b) as being unpatentable over Chapman et al. (USP 6,304,552) in view of Barnes et al. (USP 7,382,787) further in view of Wegner et al. (USP 6,032,192).

7. With regard to claims 1, 3, and 34-35, Chapman et al. discloses a stream routing unit **[lossy switch, Abstract]** for routing each of a plurality of input packet streams to any of a plurality of destinations, the stream routing unit comprising:

a plurality of input ports **[input ports, Abstract]** for receiving respective input streams;

a plurality of output ports **[output ports, Abstract]** associated with respective destinations to which the input packet streams can be routed;

storage means for holding packets of the input packet streams at addressable locations each identifiable by an address **[input buffers, col. 2, lines 4-5; the input buffers are memory spaces which hold incoming data packets until a routing decision is made as to handle the packets, col. 7, lines 50-56; these memory spaces are interpreted as either being identified as (1) physical memory addresses or (2) pointers to the packet's location in the memory]**;

an assignment data structure identifying for each input stream at least one destination to which each input packet stream is to be routed **[switch fabric, col. 3, lines 34; col. 6, lines 6-21 (interpreted as a matrix--claim 3); the switch fabric is controlled by controller 308 which identifies each stream—using the mapping table—which is headed (routed) to a particular output port, col. 8, lines 14-24]**; and

a packet allocation data structure holding for each new incoming packet a source identifier identifying the origin of the packet and the address in the storage means where the packet is held, the packet allocation data structure further holding information identifying the *output ports associated with the* intended *destination*s of *a held* packet*, the information being* derived from the assignment data structure **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; it is well known in a memory-mapping scheme that the location/address (within the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers; for example, the destination is read from the header of the packet, the routing table indicates the packets' delivery address, then the switches' input and output ports are used to derive the entry (source identifier) and exit (destination) transport node addresses which deliver the packet to the proper access point router, col. 10, lines 50-63; thus, a memory address or memory pointer (where the packet is held) must necessarily be used to perform these functions. As a second example (col. 8, lines 38-57), by mapping incoming packets to egress queues/ports, it is well known that the memory is using write/read memory pointers; interpreted as the situation where the controller transmits HI priority packets first (availability through a specific port), then, if possible, transmits LO priority packets (availability on the same port or a different port), col. 10, lines 16-24 (the algorithm prioritizes HI priority packets over LO priority packets; it transmits HI priority packets in the order they are received—claim 34); memory management for broadcasting/multicasting is known to those in the art. This prevents unnecessary multiple memory lookups with respect to output ports which output broadcast/multicast messages.**

For example, Wegner et al. discloses a queuing mechanism that withholds broadcast delivery (controls output from the memory) until all available ports can be used effectively (interpreted as becoming open—claim 36) and then submits messages to the ports simultaneously, col. 14, line 61 to col. 15, line 10. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have used a method of selective broadcasting/multicasting which uses a memory management scheme that limits memory lookups in order to provide simultaneous broadcast/multicast delivery].

The input buffers are memory spaces which hold incoming data packets until a routing decision is made as to handle the packets **[col. 7, lines 50-56]**. These memory spaces are interpreted as either being identified as (1) physical memory addresses or (2) pointers to the packet's location in the memory. Additionally, such a memory management scheme is well known to those in the art. For example, Barnes et al. (USP 7,382,787) discloses the use of a memory management scheme capable of performing additional functions on packets within a router and then having to locate the packets for output processing using memory pointers, link lists, link list arrays, etc. **[col. 3, lines 8-22]**. Thus, it would have been obvious to use a memory management scheme disclosed in Barnes et al. on the FIFOs in Chapman et al. to perform packet functions and then be able to identify the packet by address/address pointer in order to perform read/write functions in order to transmit the packet stream in the correct order and to send the stream to the correct output port.

8. With regard to claim 2, Chapman et al. discloses that the input packet streams have a lower bit rate than output streams into which they are merged at the plurality of output

ports **[the input rates are much lower than the output rates, col. 2, lines17-24; especially with bandwidth throttling mechanism, col. 9, lines 2-10; as well as sending HI and LO priority packets (col. 9, lines 28-39)]**.

9. With regard to claim 4, Chapman et al. discloses that the packet allocation data structure is an array of slots, each slot holding a source identifier and associated address [**a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; it is well known in a memory-mapping scheme that the location/address (within the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers; for example, the destination is read from the header of the packet, the routing table indicates the packets' delivery address, then the switches' input and output ports are used to derive the entry (source identifier) and exit (destination) transport node addresses which deliver the packet to the proper access point router, col. 10, lines 50-63; thus, a memory address or memory pointer (where the packet is held) must necessarily be used to perform these functions**].

10. With regard to claim 5, Chapman et al. discloses that the packet allocation data structure is associated with a write pointer which is configured to point to the next available slot in the array for the source identifier and address of the next incoming packet [**a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; by mapping incoming packets to egress queues/ports, it is well known that the memory is using write/read memory pointers;**

interpreted as the situation where the controller transmits HI priority packets first (through a specific port), then, if possible, transmits LO priority packets (the same port or a different port), col. 10, lines 16-24].

11. With regard to claims 6 and 32-33, Chapman et al. discloses that information identifying the *output ports associated with the* intended destination of the *held* packet is provided by a set of destination pointers, each destination pointer associated with a respective output port and each destination pointer being configured to point to a slot in the array which holds a source identifier and address of a packet intended for a particular destination associated with a particular output port [**a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; For example (col. 8, lines 38-57), by mapping incoming packets to egress queues/ports, it is well known that the memory is using write/read memory pointers; interpreted as the situation where the controller transmits HI priority packets first (availability through a specific port), then, if possible, transmits LO priority packets (availability on the same port or a different port), col. 10, lines 16-24 (the algorithm prioritizes HI priority packets over LO priority packets—claim 32; it transmits HI priority packets in the order they are received); memory management for broadcasting/multicasting is known to those in the art. This prevents unnecessary multiple memory lookups with respect to output ports which output broadcast/multicast messages. Wegner et al. discloses a queuing mechanism that withholds broadcast delivery (controls output from the memory—claim 33) until all available ports**

can be used effectively (interpreted as becoming open) and then submits messages to the ports simultaneously, col. 14, line 61 to col. 15, line 10].

12. With regard to claim 7, Chapman et al. discloses that the packets of a said input stream are of a common length **[interpreted as common length IP packets, col. 5, lines 62-67]**.

13. With regard to claim 8, Chapman et al. discloses a data communication system **[network, col. 1, lines 36-38]** for routing incoming packets to at least one destination, the system comprising:

a plurality of packet stream sources each generating a packet stream **[multiple input sources for each input port (connects to other users, switches, network elements, col. 5, lines 61-62]**; a stream routing unit **[lossy switch, Abstract]** comprising:

a plurality of input ports **[input ports, Abstract]** for receiving respective input streams;

a plurality of output ports **[output ports, Abstract]** associated with respective destinations to which the input packet streams can be routed;

storage means for holding packets of the input packet streams at addressable locations each identifiable by an address **[input buffers, col. 2, lines 4-5; the input buffers are memory spaces which hold incoming data packets until a routing decision is made as to handle the packets, col. 7, lines 50-56; these memory spaces are interpreted as either being identified as (1) physical memory addresses or (2) pointers to the packet's location in the memory]**;

an assignment data structure identifying for each input stream at least one destination to which each input packet stream is to be routed **[switch fabric, col. 3, lines 34; col. 6, lines 6-2; the switch fabric is controlled by controller 308 which identifies each stream—using the mapping table—which is headed (routed) to a particular output port, col. 8, lines 14-24]**; and

a packet allocation data structure holding for each new incoming packet a source identifier identifying the origin of the packet and the address in the storage means where the packet is held, the packet allocation data structure further holding information identifying the *output ports associated with the* intended *destination*s of *a held* packet*, the information being* derived from the assignment data structure **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; it is well known in a memory-mapping scheme that the location/address (within the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers; for example, the destination is read from the header of the packet, the routing table indicates the packets' delivery address, then the switches' input and output ports are used to derive the entry (source identifier) and exit (destination) transport node addresses which deliver the packet to the proper access point router, col. 10, lines 50-63; thus, a memory address or memory pointer (where the packet is held) must necessarily be used to perform these functions; As a second example (col. 8, lines 38-57), by mapping incoming packets to egress queues/ports, it is well known that the memory is using write/read memory pointers; interpreted as the situation where the**

controller transmits HI priority packets first (availability through a specific port), then, if possible, transmits LO priority packets (availability on the same port or a different port), col. 10, lines 16-24; memory management for broadcasting/multicasting is known to those in the art. This prevents unnecessary multiple memory lookups with respect to output ports which output broadcast/multicast messages. For example, Wegner et al. discloses a queuing mechanism that withholds broadcast delivery until all available ports can be used effectively and then submits messages to the ports simultaneously, col. 14, line 61 to col. 15, line 10. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have used a method of selective broadcasting/multicasting which uses a memory management scheme that limits memory lookups in order to provide simultaneous broadcast/multicast delivery];

and

a plurality of destinations for receiving packets of the packet streams generated by the sources **[multiple outputs for each output port (connects to other users, switches, network elements, col. 5, lines 61-62]**.

The input buffers are memory spaces which hold incoming data packets until a routing decision is made as to handle the packets **[col. 7, lines 50-56]**. These memory spaces are interpreted as either being identified as (1) physical memory addresses or (2) pointers to the packet's location in the memory. Additionally, such a memory management scheme is well known to those in the art. For example, Barnes et al. (USP 7,382,787) discloses the use of a memory management scheme capable of performing additional functions on packets within a

router and then having to locate the packets for output processing using memory pointers, link lists, link list arrays, etc. **[col. 3, lines 8-22]**. Thus, it would have been obvious to use a memory management scheme disclosed in Barnes et al. on the FIFOs in Chapman et al. to perform packet functions and then be able to identify the packet by address/address pointer in order to perform read/write functions in order to transmit the packet stream in the correct order and to send the stream to the correct output port.

14. With regard to claim 9, Chapman et al. discloses that at least one of the destinations comprises a programmable transport interface **[interpreted as a repeater, col. 12, lines 15-28]**.

15. With regard to claim 10, Chapman et al. discloses that the input packet streams have a lower bit rate than output streams into which they are merged at the plurality of output ports **[the input rates are much lower than the output rates, col. 2, lines17-24; especially with bandwidth throttling mechanism, col. 9, lines 2-10; as well as sending HI and LO priority packets (col. 9, lines 28-39)]**.

16. With regard to claim 11, Chapman et al. discloses a method of routing packet streams **[Abstract]** from a plurality of sources to any of a plurality of destinations, the method comprising:

receiving said packet streams **[multiple input sources for each input port (connects to other users, switches, network elements, col. 5, lines 61-62]**;

identifying for each input packet stream at least one destination to which each input packet stream is to be routed using an assignment data structure **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; it is well known in a memory-mapping scheme that the location/address (within the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers; for example, the destination is read from the header of the packet, the routing table indicates the packets' delivery address, then the switches' input and output ports are used to derive the entry (source identifier) and exit (destination) transport node addresses which deliver the packet to the proper access point router, col. 10, lines 50-63; thus, a memory address or memory pointer (where the packet is held) must necessarily be used to perform these functions]**;

holding each packet of the packet stream *in a storage means* at an addressable location identifiable by an address in *that* storage means **[input buffers, col. 2, lines 4-5; the input buffers are memory spaces which hold incoming data packets until a routing decision is made as to handle the packets, col. 7, lines 50-56; these memory spaces are interpreted as either being identified as (1) physical memory addresses or (2) pointers to the packet's location in the memory]**;

holding for each new incoming packet *a packet allocation data structure which stores* a source identifier identifying the origin of the packet and the address in the storage means where the packet is held [**a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-5; it is well known in a memory-mapping scheme that the location/address (within**

the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers; for example, the destination is read from the header of the packet, the routing table indicates the packets' delivery address, then the switches' input and output ports are used to derive the entry (source identifier) and exit (destination) transport node addresses which deliver the packet to the proper access point router, col. 10, lines 50-63; thus, a memory address or memory pointer (where the packet is held) must necessarily be used to perform these functions];

holding information *in an assignment data structure* identifying the intended destination of the packet derived from the assignment data structure [**a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; it is well known in a memory-mapping scheme that the location/address (within the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers; for example, the destination is read from the header of the packet, the routing table indicates the packets' delivery address, then the switches' input and output ports are used to derive the entry (source identifier) and exit (destination) transport node addresses which deliver the packet to the proper access point router, col. 10, lines 50-63; thus, a memory address or memory pointer (where the packet is held) must necessarily be used to perform these functions]**;

using said *assignment data structure* information identifying the intended destination to *further include in the packet allocation data structure information identifying output ports associated with intended destinations of the held packet; routing* the packet from the storage means to the or each output port **[output ports, Abstract]** associated with the respective

identified destination(s) [**a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; for example, the destination is read from the header of the packet, the routing table indicates the packets' delivery address, then the switches' input and output ports are used to derive the entry (source identifier) and exit (destination) transport node addresses which deliver the packet to the proper access point router, col. 10, lines 50-63; thus, a memory address or memory pointer (where the packet is held) must necessarily be used to perform these functions; As a second example (col. 8, lines 38-57), by mapping incoming packets to egress queues/ports, it is well known that the memory is using write/read memory pointers; interpreted as the situation where the controller transmits HI priority packets first (availability through a specific port), then, if possible, transmits LO priority packets (availability on the same port or a different port), col. 10, lines 16-24 (the algorithm prioritizes HI priority packets over LO priority packets; it transmits HI priority packets in the order they are received); memory management for broadcasting/multicasting is known to those in the art. This prevents unnecessary multiple memory lookups with respect to output ports which output broadcast/multicast messages. For example, Wegner et al. discloses a queuing mechanism that withholds broadcast delivery (controls output from the memory) until all available ports can be used effectively (interpreted as becoming open) and then submits messages to the ports simultaneously, col. 14, line 61 to col. 15, line 10. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have used a method of selective broadcasting/multicasting which uses a

memory management scheme that limits memory lookups in order to provide simultaneous broadcast/multicast delivery].

The input buffers are memory spaces which hold incoming data packets until a routing decision is made as to handle the packets **[col. 7, lines 50-56]**. These memory spaces are interpreted as either being identified as (1) physical memory addresses or (2) pointers to the packet's location in the memory. Additionally, such a memory management scheme is well known to those in the art. For example, Barnes et al. (USP 7,382,787) discloses the use of a memory management scheme capable of performing additional functions on packets within a router and then having to locate the packets for output processing using memory pointers, link lists, link list arrays, etc. **[col. 3, lines 8-22]**. Thus, it would have been obvious to use a memory management scheme disclosed in Barnes et al. on the FIFOs in Chapman et al. to perform packet functions and then be able to identify the packet by address/address pointer in order to perform read/write functions in order to transmit the packet stream in the correct order and to send the stream to the correct output port.

17. With regard to claim 12, Chapman et al. discloses that the input packet streams have a lower bit rate than output streams into which they are merged at the output ports **[the input rates are much lower than the output rates, col. 2, lines 17-24; especially with bandwidth throttling mechanism, col. 9, lines 2-10; as well as sending HI and LO priority packets (col. 9, lines 28-39)]**.

18. With regard to claim 13, Chapman et al. discloses that the information identifying the *output ports associated with the* intended destination of the *held* packet is provided by a set of destination pointers, said method further comprising:

associating each destination pointer with a respective output port; and configuring each destination pointer to point to a source identifier and address of a packet intended for the destination associated with that output port [**a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; by mapping incoming packets to egress queues/ports, it is well known that the memory is using write/read memory pointers; for example, the destination is read from the header of the packet, the routing table indicates the packets' delivery address, then the switches' input and output ports are used to derive the entry (source identifier) and exit (destination) transport node addresses which deliver the packet to the proper access point router, col. 10, lines 50-63; thus, a memory address or memory pointer (where the packet is held) must necessarily be used to perform these functions; As a second example (col. 8, lines 38-57), by mapping incoming packets to egress queues/ports, it is well known that the memory is using write/read memory pointers; interpreted as the situation where the controller transmits HI priority packets first (availability through a specific port), then, if possible, transmits LO priority packets (availability on the same port or a different port), col. 10, lines 16-24 (the algorithm prioritizes HI priority packets over LO priority packets; it transmits HI priority packets in the order they are received); memory management for broadcasting/multicasting is known to those in the art. This prevents unnecessary multiple memory lookups with respect to output ports which output**

broadcast/multicast messages. For example, Wegner et al. discloses a queuing mechanism that withholds broadcast delivery (controls output from the memory) until all available ports can be used effectively (interpreted as becoming open) and then submits messages to the ports simultaneously, col. 14, line 61 to col. 15, line 10.].

19. With regard to claim 14, Chapman et al. discloses holding each new incoming packet in a packet allocation data structure having a plurality of slots;

holding in each slot a source identifier and associated address; and associating each slot with a write pointer which is configured to point to the next available slot in the array for the source identifier and address of the next incoming packet [**a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; for example (col. 8, lines 38-57), by mapping incoming packets to egress queues/ports, it is well known that the memory is using write/read memory pointers; interpreted as the situation where the controller transmits HI priority packets first (availability through a specific port), then, if possible, transmits LO priority packets (availability on the same port or a different port), col. 10, lines 16-24 (the algorithm prioritizes HI priority packets over LO priority packets; it transmits HI priority packets in the order they are received)**].

Chapman et al. in view of Barnes et al.

20. Claims 15-23 and 36-38 are rejected under 35 U.S.C. 102(b) as being unpatentable over Chapman et al. (USP 6,304,552) in view of Barnes et al. (USP 7,382,787).

21. With regard to claim 15, Chapman et al. discloses a device **[lossy switch, Abstract]** for delivering incoming packets to at least one destination **[Abstract]**, the device comprising:

an addressable memory which stores incoming packets at a plurality of address locations in the memory **[input buffers, col. 2, lines 4-5; the input buffers are memory spaces which hold incoming data packets until a routing decision is made as to handle the packets, col. 7, lines 50-56; these memory spaces are interpreted as either being identified as (1) physical memory addresses or (2) pointers to the packet's location in the memory]**;

a source to destination matrix for mapping at least one source to at least one destination **[switch fabric, col. 3, lines 34; col. 6, lines 6-21; interpreted as a matrix; the switch fabric is controlled by controller 308 which identifies each stream—using the mapping table—which is headed (routed) to a particular output port, col. 8, lines 14-24]**;

a packet allocation table for associating a source and at least one destination for a particular packet with *the address location in the addressable* a memory **[input buffers, col. 2, lines 4-5; the input buffers are memory spaces which hold incoming data packets until a routing decision is made as to handle the packets, col. 7, lines 50-56; these memory spaces are interpreted as either being identified as (1) physical memory addresses or (2) pointers to the packet's location in the memory]** *where* the particular packet is stored **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; it is well known in a memory-mapping**

scheme that the location/address (within the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers; for example, the destination is read from the header of the packet, the routing table indicates the packets' delivery address, then the switches' input and output ports are used to derive the entry (source identifier) and exit (destination) transport node addresses which deliver the packet to the proper access point router, col. 10, lines 50-63; thus, a memory address or memory pointer (where the packet is held) must necessarily be used to perform these functions]; and

an algorithm for controlling removal of the incoming packets from a memory to at least one destination **[packet discard, col. 11, lines 58-63]**, wherein the incoming packets have a lower bit-rate than packets delivered to the at least one destination **[the input rates are much lower than the output rates, col. 2, lines17-24; especially with bandwidth throttling mechanism, col. 9, lines 2-10; as well as sending HI and LO priority packets (col. 9, lines 28-39)]**.

The input buffers are memory spaces which hold incoming data packets until a routing decision is made as to handle the packets **[col. 7, lines 50-56]**. These memory spaces are interpreted as either being identified as (1) physical memory addresses or (2) pointers to the packet's location in the memory. Additionally, such a memory management scheme is well known to those in the art. For example, Barnes et al. (USP 7,382,787) discloses the use of a memory management scheme capable of performing additional functions on packets within a router and then having to locate the packets for output processing using memory pointers, link lists, link list arrays, etc. **[col. 3, lines 8-22]**. Thus, it would have been obvious to use a memory management scheme disclosed in Barnes et al. on the FIFOs in Chapman et al. to perform packet

functions and then be able to identify the packet by address/address pointer in order to perform read/write functions in order to transmit the packet stream in the correct order and to send the stream to the correct output port.

22. With regard to claim 16, Chapman et al. discloses a memory for holding the incoming packets at addressable locations each identifiable by an address **[FIFO buffers, col. 7, line 50 to col. 8, line 10; the input buffers are memory spaces which hold incoming data packets until a routing decision is made as to handle the packets, col. 7, lines 50-56; these memory spaces are interpreted as either being identified as (1) physical memory addresses or (2) pointers to the packet's location in the memory]**.

23. With regard to claim 17, Chapman et al. discloses a plurality of input ports for receiving respective input packets **[multiple input sources for each input port (connects to other users, switches, network elements, col. 5, lines 61-62]**; and

a plurality of output ports associated with respective destinations to which the input packets can be routed **[multiple outputs for each output port (connects to other users, switches, network elements, col. 5, lines 61-62]**.

24. With regard to claim 18, Chapman et al. discloses a method for delivering incoming packets to at least one destination, the method comprising:

storing incoming packets at a plurality of addressable locations in memory **[input buffers, col. 2, lines 4-5; the input buffers are memory spaces which hold incoming data**

packets until a routing decision is made as to handle the packets, col. 7, lines 50-56; these memory spaces are interpreted as either being identified as (1) physical memory addresses or (2) pointers to the packet's location in the memory];

mapping at least one source to at least one destination **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; it is well known in a memory-mapping scheme that the location/address (within the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers; for example, the destination is read from the header of the packet, the routing table indicates the packets' delivery address, then the switches' input and output ports are used to derive the entry (source identifier) and exit (destination) transport node addresses which deliver the packet to the proper access point router, col. 10, lines 50-63; thus, a memory address or memory pointer (where the packet is held) must necessarily be used to perform these functions]**;

associating a source and at least one destination for a particular packet with *the address location in* memory location **[input buffers, col. 2, lines 4-5; the input buffers are memory spaces which hold incoming data packets until a routing decision is made as to handle the packets, col. 7, lines 50-56; these memory spaces are interpreted as either being identified as (1) physical memory addresses or (2) pointers to the packet's location in the memory]** *where* the particular packet is stored **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; it is well known in a memory-mapping scheme that the location/address (within the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read**

pointers; for example, the destination is read from the header of the packet, the routing table indicates the packets' delivery address, then the switches' input and output ports are used to derive the entry (source identifier) and exit (destination) transport node addresses which deliver the packet to the proper access point router, col. 10, lines 50-63; thus, a memory address or memory pointer (where the packet is held) must necessarily be used to perform these functions]; and

controlling removal of the incoming packets from a memory to at least one destination **[packet discard, col. 11, lines 58-63]**, wherein the incoming packets have a lower bit-rate than packets delivered to the at least one destination **[the input rates are much lower than the output rates, col. 2, lines17-24; especially with bandwidth throttling mechanism, col. 9, lines 2-10; as well as sending HI and LO priority packets (col. 9, lines 28-39)]**.

The input buffers are memory spaces which hold incoming data packets until a routing decision is made as to handle the packets **[col. 7, lines 50-56]**. These memory spaces are interpreted as either being identified as (1) physical memory addresses or (2) pointers to the packet's location in the memory. Additionally, such a memory management scheme is well known to those in the art. For example, Barnes et al. (USP 7,382,787) discloses the use of a memory management scheme capable of performing additional functions on packets within a router and then having to locate the packets for output processing using memory pointers, link lists, link list arrays, etc. **[col. 3, lines 8-22]**. Thus, it would have been obvious to use a memory management scheme disclosed in Barnes et al. on the FIFOs in Chapman et al. to perform packet functions and then be able to identify the packet by address/address pointer in order to perform

read/write functions in order to transmit the packet stream in the correct order and to send the stream to the correct output port.

25. With regard to claim 19, Chapman et al. discloses holding the incoming packets at addressable locations each identifiable by an address **[FIFO buffers, col. 7, line 50 to col. 8, line 10; the input buffers are memory spaces which hold incoming data packets until a routing decision is made as to handle the packets, col. 7, lines 50-56; these memory spaces are interpreted as either being identified as (1) physical memory addresses or (2) pointers to the packet's location in the memory]**.

26. With regard to claim 20, Chapman et al. discloses receiving respective input packets **[multiple input sources for each input port (connects to other users, switches, network elements, col. 5, lines 61-62]**; and

routing outgoing packets through a plurality of output ports associated with respective destinations [**a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; by mapping incoming packets to egress queues/ports, it is well known that the memory is using write/read memory pointers; interpreted as the situation where the controller transmits HI priority packets first (through a specific port), then, if possible, transmits LO priority packets (the same port or a different port), col. 10, lines 16-24]**.

27. With regard to claim 21, Chapman et al. discloses creating a source to destination matrix **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; it is well known in a memory-mapping scheme that the location/address (within the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers; for example, the destination is read from the header of the packet, the routing table indicates the packets' delivery address, then the switches' input and output ports are used to derive the entry (source identifier) and exit (destination) transport node addresses which deliver the packet to the proper access point router, col. 10, lines 50-63; thus, a memory address or memory pointer (where the packet is held) must necessarily be used to perform these functions]**.

28. With regard to claim 22, Chapman et al. discloses that at least one destination is a programmable transport interface **[interpreted as a repeater, col. 12, lines 15-28]**.

29. With regard to claim 23, Chapman et al. discloses that the memory is an SRAM memory **[FIFO buffers, col. 7, line 50 to col. 8, line 10; also RAM memory]**.

30. With regard to claim 36, Chapman et al. discloses a stream routing unit, comprising:

a plurality of input ports **[input ports, Abstract]**, each input port receiving an input packet stream;

a plurality of output ports **[output ports, Abstract]**, each output port outputting an output packet stream;

a memory including a plurality of addressable memory locations **[input buffers, col. 2, lines 4-5; the input buffers are memory spaces which hold incoming data packets until a routing decision is made as to handle the packets, col. 7, lines 50-56; these memory spaces are interpreted as either being identified as (1) physical memory addresses or (2) pointers to the packet's location in the memory]**;

a source-to-destination matrix storing data identifying, for each source of the input packet streams coupled to the input ports, one or more destinations, for packets within those input packet streams, which are coupled to receive the output packet streams from the output ports **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; it is well known in a memory-mapping scheme that the location/address (within the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers; for example, the destination is read from the header of the packet, the routing table indicates the packets' delivery address, then the switches' input and output ports are used to derive the entry (source identifier) and exit (destination) transport node addresses which deliver the packet to the proper access point router, col. 10, lines 50-63; thus, a memory address or memory pointer (where the packet is held) must necessarily be used to perform these functions]**;

a processor for storing packets of the input packet streams in the memory and for retrieving stored packets from the memory to form the output packet streams **[Fig. 3, Controller 308]**;

the processor filling a packet allocation table which includes a plurality of slot locations, each slot location storing a source identifier which identifies a source of the received packet

stream to which a given packet belongs linked in the packet allocation table to an address in the memory for the addressable memory location where that given packet has been stored by the processor **[Controller 308 runs a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; it is well known in a memory-mapping scheme that the location/address (within the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers; for example, the destination is read from the header of the packet, the routing table indicates the packets' delivery address, then the switches' input and output ports are used to derive the entry (source identifier) and exit (destination) transport node addresses which deliver the packet to the proper access point router, col. 10, lines 50-63; thus, a memory address or memory pointer (where the packet is held) must necessarily be used to perform these functions]**;

a destination pointer, associated with each one of the output ports, implemented by the processor for pointing to a slot location in the packet allocation table from which the address of the given packet is retrieved, the destination pointer pointing to the slot location in accordance with the destination data stored in the source-to-destination matrix **[Controller 308 runs a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; it is well known in a memory-mapping scheme that the location/address (within the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers; for example, the destination is read from the header of the packet, the routing table indicates the packets' delivery address, then the switches' input and output ports are used to derive the entry (source**

identifier) and exit (destination) transport node addresses which deliver the packet to the proper access point router, col. 10, lines 50-63; thus, a memory address or memory pointer (where the packet is held) must necessarily be used to perform these functions];

the processor retrieving the given packet from the memory at the address provided in the slot location pointed at by the destination pointer, sending the retrieved given packet to each output port associated with the destination that is linked in the source-to-destination matrix with the source identified in the slot location for inclusion in the output packet stream of the output port **[Controller 308 runs a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; it is well known in a memory-mapping scheme that the location/address (within the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers; for example, the destination is read from the header of the packet, the routing table indicates the packets' delivery address, then the switches' input and output ports are used to derive the entry (source identifier) and exit (destination) transport node addresses which deliver the packet to the proper access point router, col. 10, lines 50-63; thus, a memory address or memory pointer (where the packet is held) must necessarily be used to perform these functions]**.

The input buffers are memory spaces which hold incoming data packets until a routing decision is made as to handle the packets **[col. 7, lines 50-56]**. These memory spaces are interpreted as either being identified as (1) physical memory addresses or (2) pointers to the packet's location in the memory. Additionally, such a memory management scheme is well known to those in the art. For example, Barnes et al. (USP 7,382,787) discloses the use of a

memory management scheme capable of performing additional functions on packets within a router and then having to locate the packets for output processing using memory pointers, link lists, link list arrays, etc. **[col. 3, lines 8-22]**. Thus, it would have been obvious to use a memory management scheme disclosed in Barnes et al. on the FIFOs in Chapman et al. to perform packet functions and then be able to identify the packet by address/address pointer in order to perform read/write functions in order to transmit the packet stream in the correct order and to send the stream to the correct output port.

31. With regard to claim 37, Chapman et al. discloses a write pointer implemented by the processing means for pointing to an open slot location in the packet allocation table to which the source identifier and address of the given packet are written **[Controller 308 runs a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; it is well known in a memory-mapping scheme that the location/address (within the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers; for example, the destination is read from the header of the packet, the routing table indicates the packets' delivery address, then the switches' input and output ports are used to derive the entry (source identifier) and exit (destination) transport node addresses which deliver the packet to the proper access point router, col. 10, lines 50-63; thus, a memory address or memory pointer (where the packet is held) must necessarily be used to perform these functions]**.

32. With regard to claim 38, Chapman et al. discloses that a bit rate of the input packet streams

is lower than a bit rate of the output packet streams **[the input rates are much lower than the output rates, col. 2, lines 17-24; especially with bandwidth throttling mechanism, col. 9, lines 2-10; as well as sending HI and LO priority packets (col. 9, lines 28-39)]**.

Response to Arguments

33. Applicant's arguments filed on January 20, 2009 have been fully considered but they are not persuasive.

34. With respect to claim 1, Applicants state that Chapman et al. fails to disclose, teach, or suggest addressable buffers for the incoming packet streams **[See Applicants' Amendment dated January 20, 2009, page 11, paragraphs 4-5]**. Applicants argue, apparently, that the input buffers of Chapman et al. are limited to FIFOs 320/324 and further explain, apparently, that (a) the well understood FIFO architecture and (b) addressable buffers are mutually exclusive **[See Applicants' Amendment dated January 20, 2009, page 11, paragraph 6]**. Specifically, Applicants argue, apparently, that Chapman et al. must contain explicit motivation for having addressable buffers and the absence of such explicit motivation shows that such a modification would not have been obvious to one of ordinary skill in the art at the time of the invention **[See Applicants' Amendment dated January 20, 2009, page 11, paragraph 6 to page 12, paragraph 2]**. Applicants further argue, apparently, that there is no explicit motivation to replace the addressable buffers of Chapman et al. with the memory management scheme in Barnes et al. **[See Applicants' Amendment dated January 20, 2009, page 12, paragraphs 3-**

4]. Applicants make similar arguments for independent claims 8, 11, 15, and 18 **[See Applicants' Amendment dated January 20, 2009, page 14, paragraph 5 to page 15, paragraph 2]**. The examiner respectfully disagrees.

35. First, as noted in the rejection of claim 1 above, Chapman et al. discloses that the input buffers are memory spaces which hold incoming data packets until a routing decision is made as to handle the packets **[col. 7, lines 50-56]**. These memory spaces are interpreted as either being identified as (1) physical memory addresses or (2) pointers to the packet's location in the memory. Additionally, such a memory management scheme is well known to those in the art. For example, Barnes et al. (USP 7,382,787) discloses the use of a memory management scheme capable of performing additional functions on packets within a router and then having to locate the packets for output processing using memory pointers, link lists, link list arrays, etc. **[col. 3, lines 8-22]**. Thus, it would have been obvious to use a memory management scheme disclosed in Barnes et al. on the FIFOs in Chapman et al. to perform packet functions and then be able to identify the packet by address/address pointer in order to perform read/write functions in order to transmit the packet stream in the correct order and to send the stream to the correct output port.

36. Second, contrary to Applicants statement that addressing locations in a FIFO buffer is unnecessary, Chapman et al. further discloses that memory 310 implements queue mechanisms to accept data from the input ports **[col. 8, lines 11-24]**. Memory is merely the medium on which the buffers are created—the actual created [and deleted] and management of the buffers is controlled by controller 308 **[*See Id.*]**. Thus, buffers 320/324 used in this type of memory

management scheme [input buffers 320/324 and memory 310] must necessarily use either (1) physical memory addresses or (2) pointers to the packet's location in the memory.

37. *Arguendo*, even if buffers 320/324 of Chapman et al. were limited to a non-addressable first-in, first-out scheme, Chapman et al. still employs addressable queues at the input side of the switch [before being transported through the switch fabric] through the use of input queues created within memory 310 **[col. 8, lines 11-24]**. Even if one were able to divest Chapman et al. of the already-disclosed addressable input queues **[col. 7, lines 50-56]**, such a memory management scheme is well known to those in the art. For example, Barnes et al. (USP 7,382,787) discloses the use of a memory management scheme capable of performing additional functions on packets within a router and then having to locate the packets for output processing using memory pointers, link lists, link list arrays, etc. **[col. 3, lines 8-22]**. Thus, it would have been obvious to use a memory management scheme disclosed in Barnes et al. on the FIFOs in Chapman et al. to perform packet functions and then be able to identify the packet by address/address pointer in order to perform read/write functions in order to transmit the packet stream in the correct order and to send the stream to the correct output port.

38. Third, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

39. Fourth, in response to applicant's argument that explicit motivation for an addressable input memory scheme is absent from either reference, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In this case, Chapman et al. discloses an addressable queuing mechanism on the input side of the switch **[col. 7, lines 50-56]**. And, even absent such an addressable input queuing mechanism, such a memory management scheme is well known to those in the art. For example, Barnes et al. (USP 7,382,787) discloses the use of a memory management scheme capable of performing additional functions on packets within a router and then having to locate the packets for output processing using memory pointers, link lists, link list arrays, etc. **[col. 3, lines 8-22]**. Thus, it would have been obvious to use a memory management scheme disclosed in Barnes et al. on the FIFOs in Chapman et al. to perform packet functions and then be able to identify the packet by address/address pointer in order to perform read/write functions in order to transmit the packet stream in the correct order and to send the stream to the correct output port.

40. Fifth, ***KSR*** has foreclosed the issue of explicit disclosure within a reference(s) to provide the motivation to combine such a reference with other references as well an explicit rationale(s) for making obvious changes to the prior art.

41. With respect to claim 1, Applicants state that Chapman et al. fails to disclose, teach, or suggest a packet allocation data structure which hold the packet' s source identifier and the address where such a packet is stored **[See Applicants' Amendment dated January 20, 2009, page 13, paragraphs 1-3]**. Applicants have requested that the examiner make explicit through the use of a prior art reference what is considered to be well-known in the art **[See Applicants' Amendment dated January 20, 2009, page 13, paragraph 3]**.

42. Gaudet et al. (USP 6,421,348), discloses a data exchanger which monitors the Source ID and places cells in identified/identifiable memory locations of an associated buffer **[col. 7, lines 28-38]**.

43. With respect to claim 1, Applicants state that Chapman et al. does not explicitly disclose a "data structure" **[See Applicants' Amendment dated January 20, 2009, page 14, paragraph 2]**. The examiner has interpreted this argument to mean that Applicants are arguing, apparently, that a "data structure" is different than the cited routing table **[See Applicants' Amendment dated January 20, 2009, page 14, paragraph 2]**. The examiner respectfully disagrees.

44. First, as noted in the rejection of claim 1 above, a routing table for mapping destination address of incoming packets to the output port **[col. 7, lines 65-67]**. It holds the source address **[col. 10, lines 5-12]**. Moreover, it is well known in a memory-mapping scheme that the location/address (within the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers. For example, the destination is read from the header of the

packet, the routing table indicates the packets' delivery address, then the switches' input and output ports are used to derive the entry (source identifier) and exit (destination) transport node addresses which deliver the packet to the proper access point router **[col. 10, lines 50-63]**. Thus, a memory address or memory pointer (where the packet is held) must necessarily be used to perform these functions. As a second example **(col. 8, lines 38-57)**, by mapping incoming packets to egress queues/ports, it is well known that the memory is using write/read memory pointers. This is interpreted as the situation where the controller transmits HI priority packets first (availability through a specific port), then, if possible, transmits LO priority packets (availability on the same port or a different port) **[col. 10, lines 16-24; (the algorithm prioritizes HI priority packets over LO priority packets; it transmits HI priority packets in the order they are received)]**. Memory management for broadcasting/multicasting is known to those in the art. This prevents unnecessary multiple memory lookups with respect to output ports which output broadcast/multicast messages. For example, Wegner et al. discloses a queuing mechanism that withholds broadcast delivery (controls output from the memory) until all available ports can be used effectively (interpreted as becoming open) and then submits messages to the ports simultaneously **[col. 14, line 61 to col. 15, line 10]**. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have used a method of selective broadcasting/multicasting which uses a memory management scheme that limits memory lookups in order to provide simultaneous broadcast/multicast delivery.

The input buffers are memory spaces which hold incoming data packets until a routing decision is made as to handle the packets **[col. 7, lines 50-56]**. These memory spaces are interpreted as either being identified as (1) physical memory addresses or (2) pointers to the

packet's location in the memory. Additionally, such a memory management scheme is well known to those in the art. For example, Barnes et al. (USP 7,382,787) discloses the use of a memory management scheme capable of performing additional functions on packets within a router and then having to locate the packets for output processing using memory pointers, link lists, link list arrays, etc. **[col. 3, lines 8-22]**. Thus, it would have been obvious to use a memory management scheme disclosed in Barnes et al. on the FIFOs in Chapman et al. to perform packet functions and then be able to identify the packet by address/address pointer in order to perform read/write functions in order to transmit the packet stream in the correct order and to send the stream to the correct output port.

45. Second, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., that a "data structure" is different than the cited routing table) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

46. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

47. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

48. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARK A. MAIS whose telephone number is (571)272-3138. The examiner can normally be reached on M-Th 9am-8pm.

49. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wing F. Chan can be reached on 571-272-7493. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

50. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

April 21, 2009

/Mark A. Mais/

Examiner, Group Art Unit 2419

/Wing F. Chan/

Supervisory Patent Examiner, Art Unit 2419